Roll No. ..... Total Printed Pages - 8

F- 829

M.Sc. (IT) (THIRD SEMESTER) EXAMINATION, Dec. - Jan., 2021-22

(ELECTIVE IV - I)

(ADVANCE COMPUTER ARCHITECTURE)

Time : Three Hours] *[Maximum Marks:100*

Note : Attempt all sections as directed.

Section - A

(Objective/Multiple Choice Questions)

Note-Attempt all questions from this Section. Each question carries 1 mark.

1. MIMD stands for:
   (A) Multiple Instruction, Multiple Data
   (B) Single Instruction, Single Data
   (C) Multiple Instruction, Single Data
   (D) Single Instruction, Multiple Data
2. Which of the following are architectural classification?
   (A) Flynn's
   (B) Feng's
   (C) Both (A) and (B)
   (D) None of these

3. COMA stands for:
   (A) Common Memory Access
   (B) Copy Memory Architecture
   (C) Cache-Only Memory Access
   (D) None of these
4. UMA stands for:
   (A) Uniform Memory Architecture
   (B) Uniform Memory Access
   (C) Unified Memory Access
   (D) None of these
5. Hypercube is a:
   (A) Static IN
   (B) Dynamic IN
   (C) Hybrid ID
   (D) Switch IN
6. Banyan IN is an example of :
   (A) Non-blocking
   (B) Blocking
   (C) Rearrangement
   (D) None of these
7. Multistage IN uses :
   (A) Hub
   (B) Router
   (C) Bridge
   (D) Switch box

8. Which Algorithm is better choice for pipelining?
   (A) Small Algorithm
   (B) Hash Algorithm
   (C) Merge-Sort Algorithm
   (D) Quick-Sort Algorithm
9. The cost of a parallel processing is primarily determined by :
   (A) Time Complexity
   (B) Switching Complexity
   (C) Circuit Complexity
   (D) None of the above
10. A processor performing fetch or decoding of different instruction during the execution of another instruction is called_____ .
   (A) Super-scaling
   (B) Pipelining
   (C) Parallel Computation
   (D) None of these
11. Under pipeline is employed in ..... processor.
   (A) CISC
   (B) RISC
   (C) Both (A) and (B)
   (D) Hybrid

12. ..... have been developed specially for pipelined system.
   (A) Utility Software
   (B) Speedup
   (C) Optimizing Compiler
   (D) None of above
13. CISC stands for :
   (A) Computer Instruction Set Computer
   (B) Combined Instruction Set Computer
   (C) Common Instrument Set Computer
   (D) Complex Instrument Set Computer
14. Split cache is used in which of the following architecture?
   (A) RISC
   (B) CISC
   (C) VLIW
   (D) None of these
15. Unified cache is used in which of the following architecture
   (A) RISC
   (B) CISC
   (C) VLIW
   (D) None of these

16. The rate at which the problem size needs to be increased to maintain efficiency?
    (A) Isoefficiency
    (B) Efficiency
    (C) Scalability
    (D) Effectiveness
17. A multicomputer system is also called:
    (A) Loosely coupled system
    (B) Tightly coupled system
    (C) Both
    (D) None of these
18. MIPS stands for:
    (A) Million Instructions Per Season
    (B) Monthly Instructions Per Second
    (C) Million Inputs Per Second
    (D) Million Instructions Per Second
19. If computer A execute a program in 10 seconds and computer B runs the same in 15 seconds, how much faster is computer A than computer B?
    (A) 1.4 times
    (B) 1.5 times
    (C) 1 time
    (D) 0.5 times

20. In one instruction is issued in one click cycle such pipelining is known as:
    (A) Super scalar pipelining
    (B) Super pipelining
    (C) Under pipelining
    (D) Scalar pipelining

Section - B

(Very Short Answer Type Questions)

Note- Attempt all questions from this Section. Each question carries 2 marks.

1. What is UMA?
2. What is SISD? Explain with a diagram?
3. What do you mean by Static Interconnection network?
4. What is Dynamic Interconnection network?
5. What is pipelining?
6. Define MAL.
7. What is Instruction set?
8. What is CISC?
9. Explain iso efficiency?
10. What do you mean by parallel processing?

Section - C

(Short Answer Type Questions)

Note- Attempt all questions from this Section. Each question carries 3 marks.

1. Explain MISD architecture with diagrams.
2. Explain NUMA and NORMA models with suitable diagrams.

3. Design a three stage 8 × 8 banyan network.
4. What is hypercube interconnection network?
5. What is scalar propelling? Explain with a diagram.
6. What is under pipelining?
7. Explain VLIW architecture with diagram.
8. Give the diagram of RISC architecture.
9. What is speed up?
10. Explain sequential and parallel programs. Give examples.

Section - D

(Long Answer Type Questions)

Note- Attempt all questions from this Section. Each question carries 6 marks.

1. What do you mean by Multiprocessor System? Explain with a suitable diagram.

Or

What is Multicomputer System? Explain with a suitable diagram.

2. Perform matrix addition of $A=\begin{bmatrix}1 & 2\\ 3 & 4\end{bmatrix}$ and $B=\begin{bmatrix}4 & 5\\ 6 & 7\end{bmatrix}$ using hypercube.

Or

What is Multistage Interconnection network? Explain in details.

3. Calculate CPI, IPC and MIPS of the super scalar super pipelining for 3 instructions when processor frequency is 100Hz.

Or

Suppose a computer without pipelining takes 15 clock cycles and a computer with pipelining take 7 clock cycles then what is speedup?

4. Differentiate between RISC and CISC architecture.

Or

Explain various functional organization of IBM 360/91 architecture.

5. Explain the parallel algorithm of matrix addition.

Or

Explain PRAM model in brief.